Amendment Under 37 C.F.R. § 1.312 U.S. Patent Application No.: 10/668,349

AMENDMENTS TO THE SPECIFICATION

Please replace the present title with the following amended title:

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Atty. Docket No.: Q76865

SOI MOSFET

Amendment Under 37 C.F.R. § 1.312

U.S. Patent Application No.: 10/668,349 Atty. Docket No.: Q76865

Please replace the paragraph no. 3, beginning on page 1, with the following amended paragraph:

In the conventional SOI transistor, an SOI substrate has a silicon substrate 101, an insulating film 102 on the silicon substrate 101, and a silicon layer 103 (hereinafter, referred to as an SOI layer) on the insulating film 102. An active region is formed in the SOI layer 103, which includes a channel region 108, a source region 109 and a drain region 110. A gate electrode 105 is formed on the SOI layer 103 through a gate insulating film 104. An isolation insulating film 106 is formed on the SOI layer 103 around the active region. A well region 111 is formed under the isolation insulating film 106, into which impurity with the same conductivity type as in the channel region 108 is introduced. A body contact 107 is formed on a predetermined area of the well region 111 to penetrate the isolation insulating film 106. Contact holes 113 are formed in the interlayer insulating film 112 to reach the source and drain regions 109 and 110. Wiring layers 114 are formed to fill the contact holes 113. A wiring layer 115 is formed on the body contact 107 to electrically connect to the well region 111. This structure is characterized in that excess carriers in the channel region 108 can escape out of the SOI transistor through the well region 111, resulting in suppression of the floating body effects. Such a path through which excess carriers can escape from the channel region 108 is referred to as a "carrier path", hereinafter.